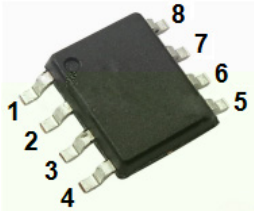


/ Descriptions			
BRCM24C02SC	SOP-8	2 Kbit	I ² C

/ Features			
1.7V	2.5~5.5V	1Mhz	1.7~2.5V
400Khz			
CMOS	400uA	1.6mA	
8			
128			
5ms			
100	100	ESD HBM	6KV
+/-200mA;			

/ Applications

/ Pinning



/ Pinning

Pin	Name	Type	Description
1	E0	Input	
2	E1	Input	
3	E2	Input	
4	GND	Ground	
5	SDA	I/O	/
6	SCL	Input	
7	WCB	Input	
8	VCC	Power	

/ Marking

/ Absolute Maximum Ratings(Ta=25)

			mA
			V

/ Reliability Characteristic

		Ñ				

/ DC Electrical Characteristics(Unless otherwise specified, Vcc = 1.7V to 5.5V,
T_A = 40 C to 85 C)

		○				
		○				

/ AC Electrical Characteristics(Unless otherwise specified, Vcc = 1.7V to 5.5V,
T_A = 40 C to 85)

		≤			≤ ≤			

[illegible]

The diagram illustrates the internal architecture of the 24C02 EEPROM. It features several key components and their interconnections:

- Serial Bus Control Logic:** Receives SCL (Serial Clock Line) and SDA (Serial Data Address) signals. It manages the Start/Stop Control Logic and the High Voltage Generator.
- High Voltage Generator:** Generates high voltage for the Page Data Latch.
- Page Data Latch:** Receives data from the Serial Bus Control Logic and outputs to the EEPROM ARRAY.
- Write Control Logic:** Receives WCOL (Write Control Output) and outputs to the EEPROM ARRAY.
- Address Counter:** Receives data from the Page Data Latch and outputs to the EEPROM ARRAY.
- Slave Address Comparator:** Receives address bits A0, A1, and A2 and outputs to the EEPROM ARRAY.
- EEPROM ARRAY:** The main storage area, receiving data from the Page Data Latch, Address Counter, and Slave Address Comparator.
- Y-DECODER:** Receives address bits A0, A1, and A2 and outputs to the EEPROM ARRAY.
- Data Out/ACK:** The output line for data from the EEPROM ARRAY, which also serves as an acknowledgment (ACK) signal.
- Serial MUX:** Multiplexes the data from the EEPROM ARRAY to the Data Out/ACK line.
- Power and Ground:** The device is powered by Vcc and grounded to GND.

/ Functional Description

H / Data Input

SDA SDA SCL (1) SCL
SDA (1)

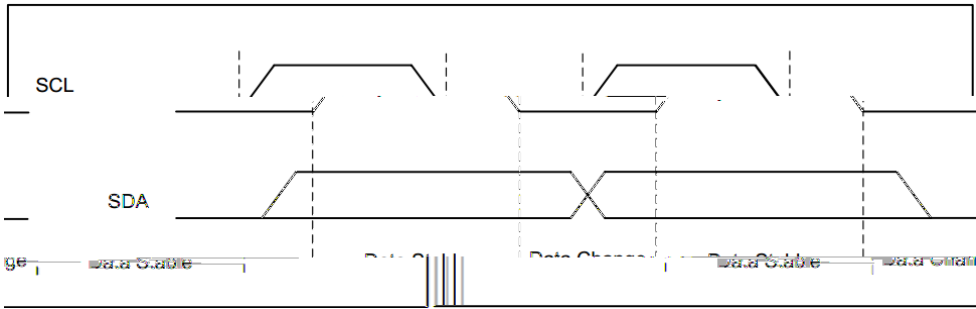


Figure 1 Data Validity

H / Start Condition

SCL SDA
2

H / Stop Condition

SCL SDA
BRCM24C02SC

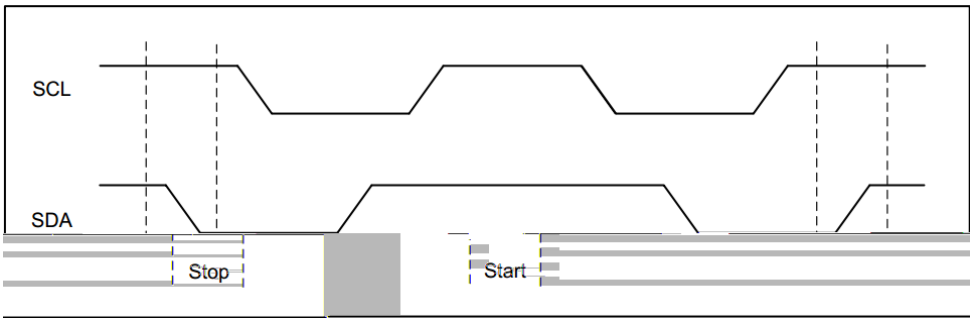


Figure 2 Start and Stop Definition

H ACK / Acknowledge

ACK BRCM24C02SC BRCM24C02SC “ 0 ”
9

/ Functional Description

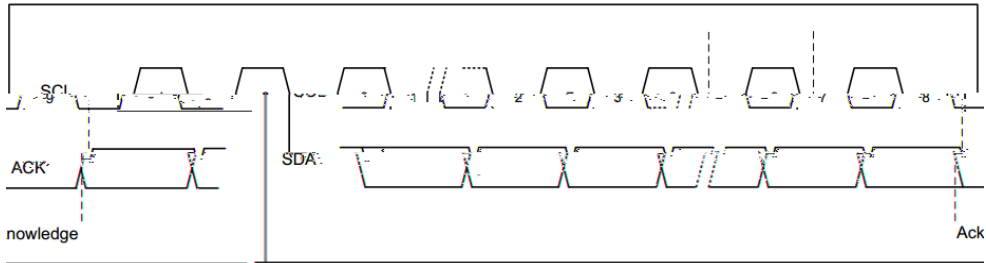


Figure 3 Output Acknowledge

H / Standby Mode

BRCM24C02SC : (a) , (b)
, (c)

H / Soft Reset

, (c) (a) , (b)
4

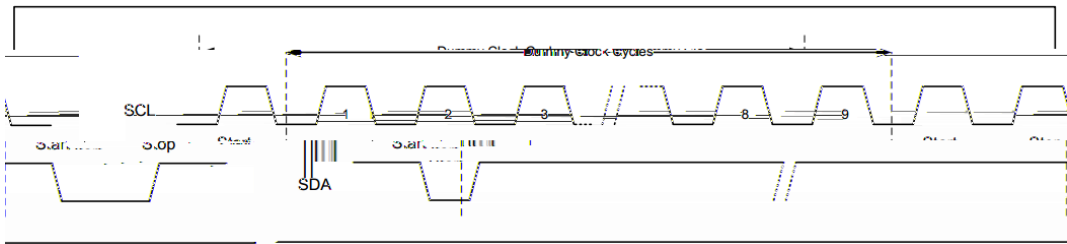


Figure 4 Soft Reset

H / Device Addressing

BRCM24C02SC 8 1
1 0

/ Functional Description

E2,E1 E0

0

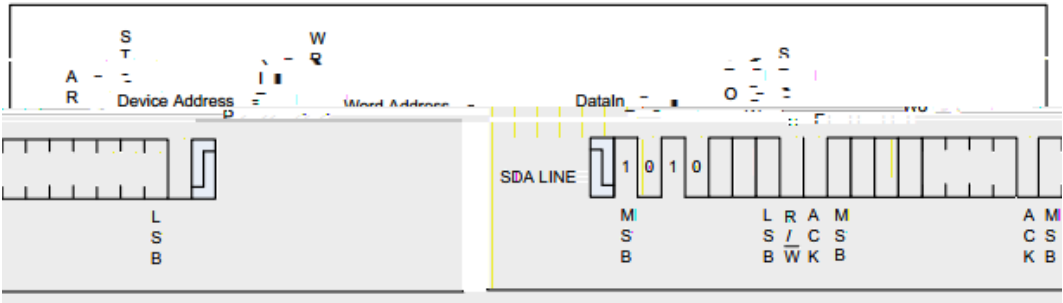
8

8 /

E2,E1 E0

0

/ Functional Description

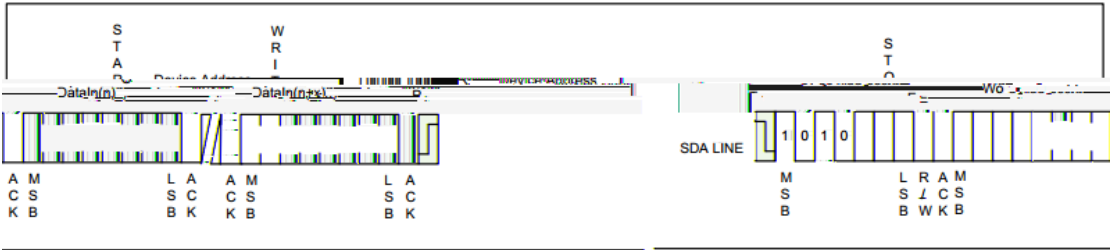


H / Page Write

BRCM24C02SC

“ 0 ”

BRCM24C02SC



/ Functional Description

H / Acknowledge Polling

BRCM24C02SC
/ BRCM24C02SC
“ 0 ”

H / Write Identification Page

16
(a) 1011b
(b) A5 / A4 0 1 A7 / A6 “ 00 ”
(c) A3 / A0
NoACK

H / Lock Identification Page

ID Lock ID
(a) 1011b;
(b) A6 1 ;
(c) xxxx xx1x x 0 1

/ Functional Description

H / Read Operations
/ “ 1 ”
;

H / Current Address Read
1
/ “ 1 ” BRCM24C02SC
“ 0 ” 7

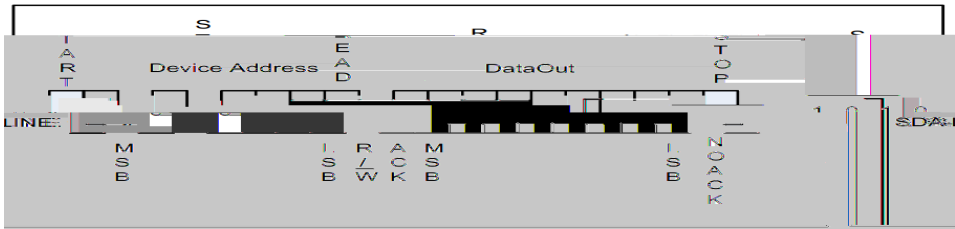


Figure 7

H / Random Address Read
“ ”
BRCM24C02SC /
BRCM24C02SC
“ 0 ” 8

/ Functional Description

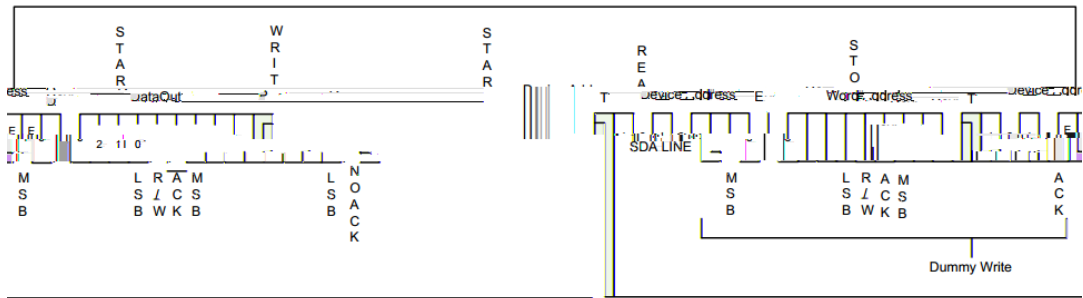


Figure 8 Random Address Read

H / Sequential Read

BRCM24C02SC

“ 0 ”

9

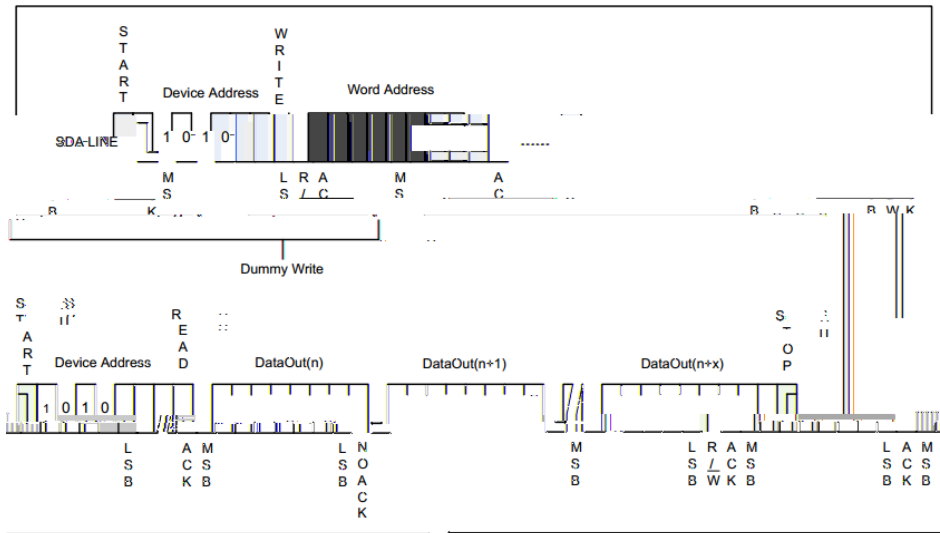
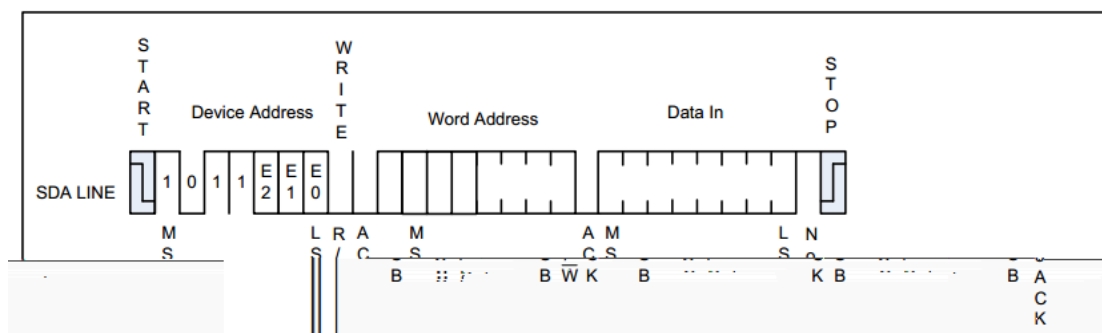


Figure 9

H / Read Identification Page

H / Read the Lock Status

$$\frac{[ACK] + [NoACK]}{10}$$


16
1
128

EEPROM

1

/ Functional Description

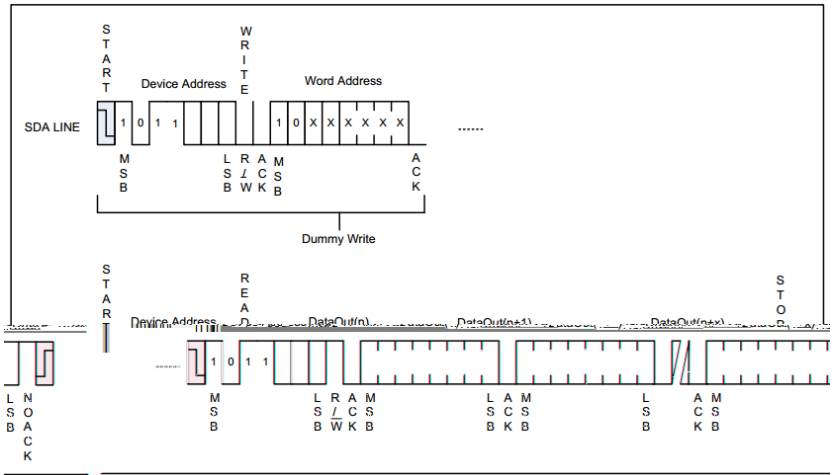
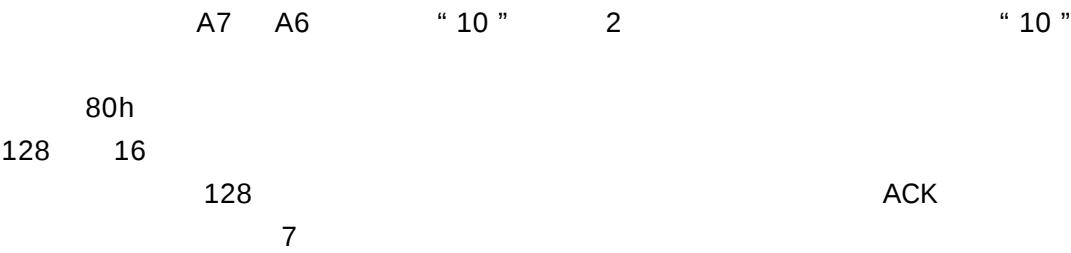
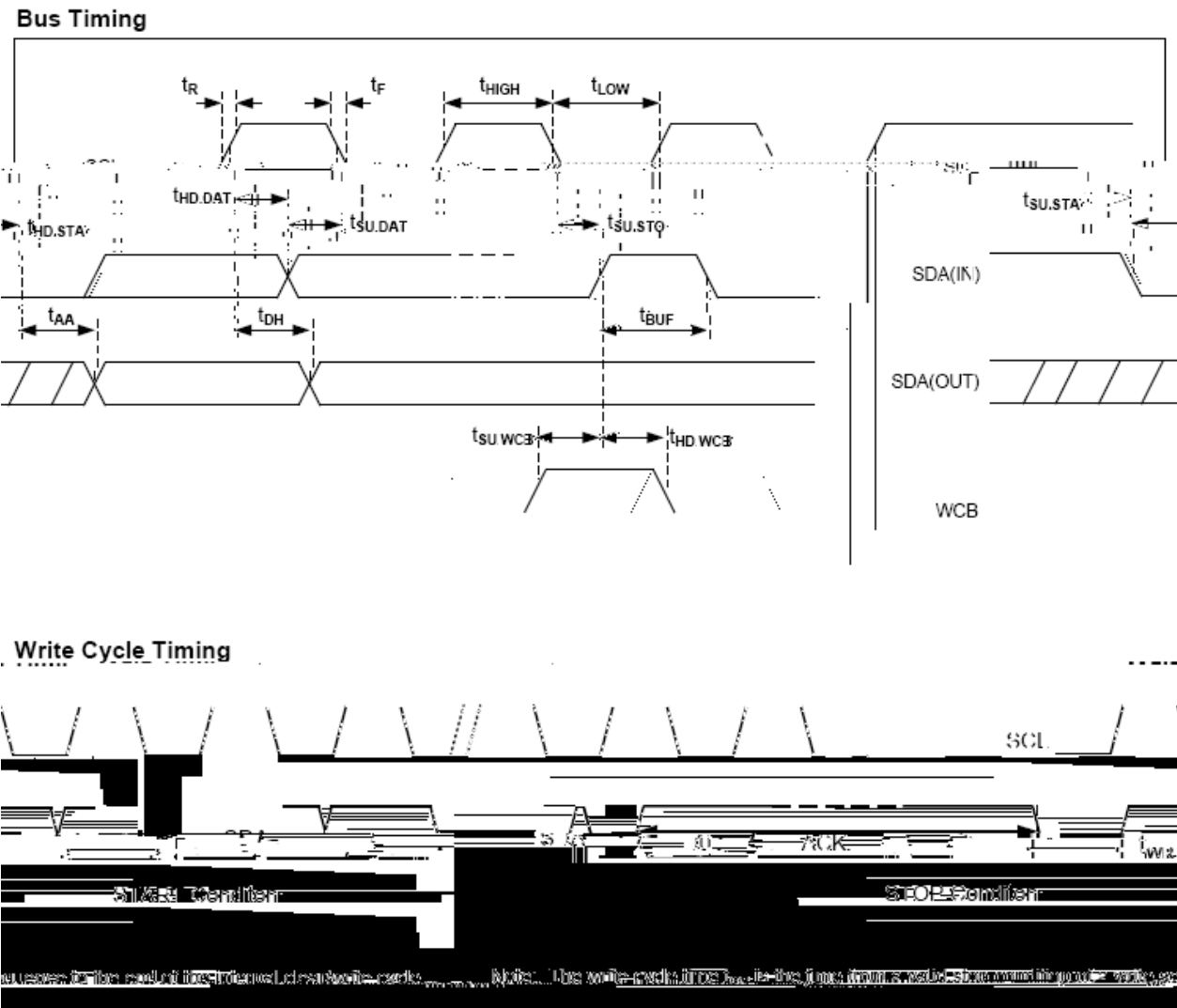


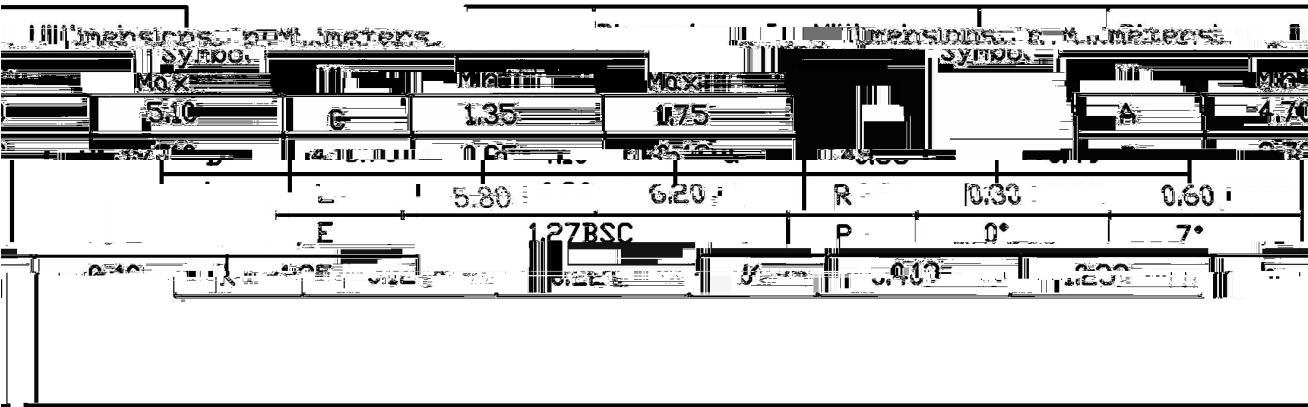
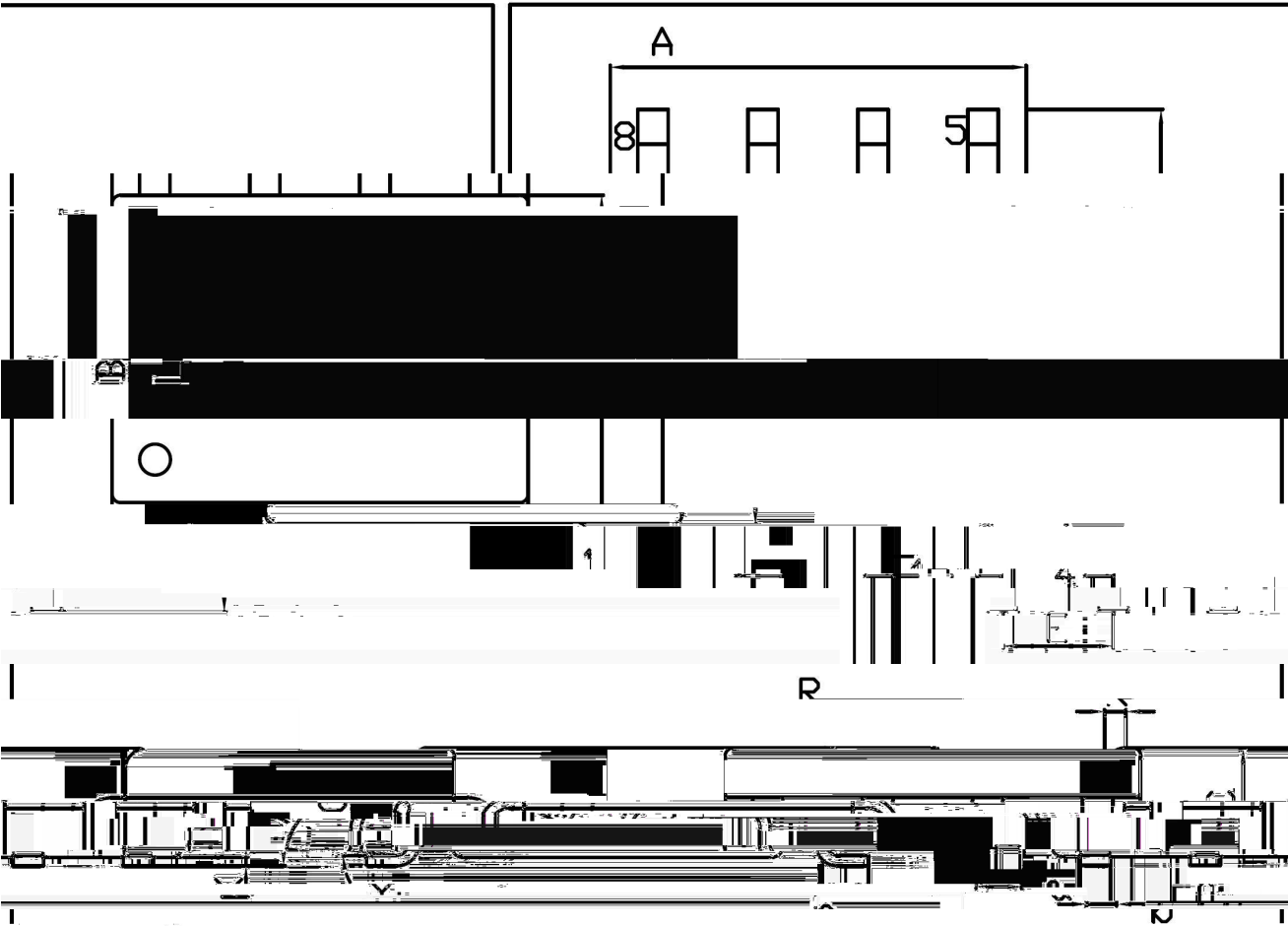
Figure 11 Sequential Read

/ Time Sequence Diagram

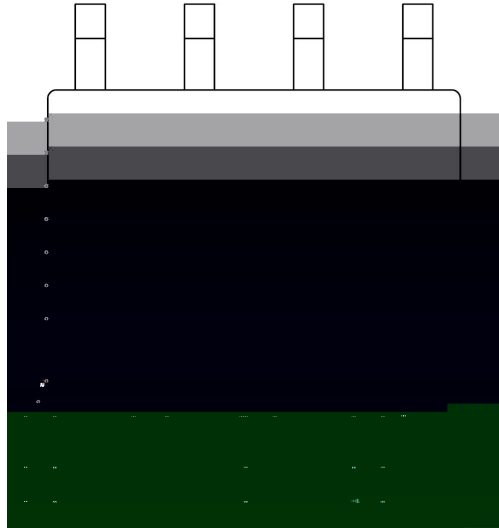


/ Package Dimensions

尺寸单位: mm

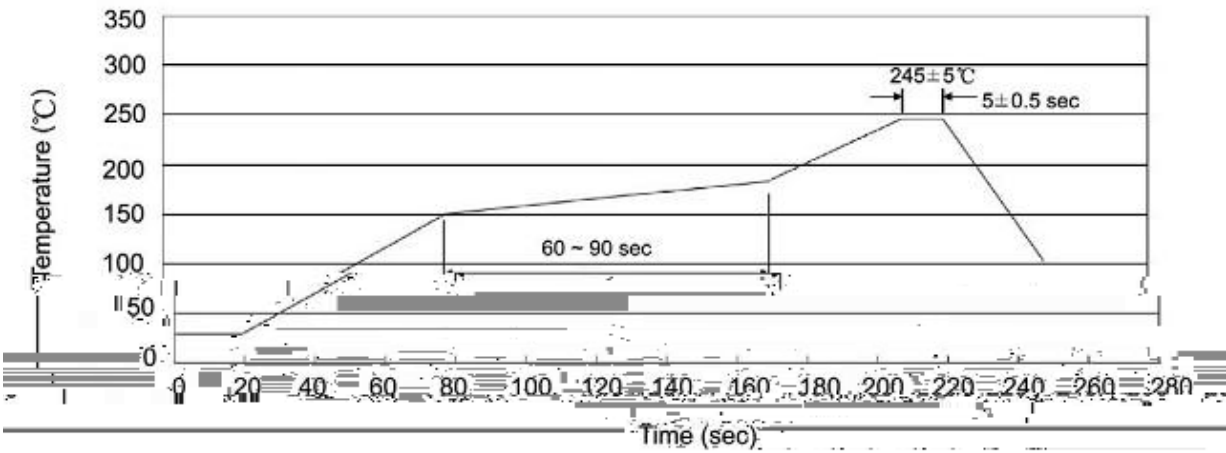


/ Marking Instructions



24C02

() /



± ± ± ±

/ Resistance to Soldering Heat Test Conditions

± ± ± ±

/ Packaging SPEC.

	Units/Reel /	Reels/Inner Box /	Units/Inner Box /	Inner Boxes/Outer Box /	Units/Outer Box /	Reel	Inner Box	Outer Box
SOP/ESOP-8	4,000	2	8,000	6	48,000	13 ×12	360×360×50	380×335×366

/ Notices